(12)

OFFICE OF NAVAL RESEARCH

GRANT N00014-89-J-1178

R&T Code 413q001-01

TECHNICAL REPORT NO. 34

# An Investigation of Si-$SiO_2$ Interface Charges in Thermally Oxidized (100), (110), (111), (511) Silicon

by

Susan C. Vitkavage and Eugene A. Irene
Department of Chemistry, CB# 3290
University of North Carolina
Chapel Hill, NC 27599-3290

Hisham Z. Massoud
Department of Electrical Engineering, Duke University
Durham, North Carolina 27706

Submitted to the
Journal of Applied Physics

SECURITY CLASSIFICATION OF THIS PAGE

# REPORT DOCUMENTATION PAGE

| | |
|---|---|
| 1a. REPORT SECURITY CLASSIFICATION<br>Unclassified | 1b. RESTRICTIVE MARKINGS |
| 2a. SECURITY CLASSIFICATION AUTHORITY | 3. DISTRIBUTION/AVAILABILITY OF REPORT<br>Approved for public release; distribution unlimited. |
| 2b. DECLASSIFICATION/DOWNGRADING SCHEDULE | |
| 4. PERFORMING ORGANIZATION REPORT NUMBER(S)<br>Technical Report #34 | 5. MONITORING ORGANIZATION REPORT NUMBER(S) |
| 6a. NAME OF PERFORMING ORGANIZATION<br>UNC Chemistry Department<br>6b. OFFICE SYMBOL (If applicable) | 7a. NAME OF MONITORING ORGANIZATION<br>Office of Naval Research (Code 413) |
| 6c. ADDRESS (City, State and ZIP Code)<br>CB# 3290, Venable Hall<br>University of North Carolina<br>Chapel Hill, NC 27599-3290 | 7b. ADDRESS (City, State and ZIP Code)<br>Chemistry Program<br>800 N. Quincy Street<br>Arlington, Virginia 22217 |
| 8a. NAME OF FUNDING/SPONSORING ORGANIZATION<br>Office of Naval Research<br>8b. OFFICE SYMBOL (If applicable) | 9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER<br>Grant #N00014-89-J-1178 |
| 8c. ADDRESS (City, State and ZIP Code)<br>Chemistry Program<br>800 N. Quincy Street, Arlington, VA 22217 | 10. SOURCE OF FUNDING NOS.<br>PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT NO. |
| 11. TITLE (Include Security Classification) AN INVESTIGATION OF Si-$SiO_2$ INTERFACE CHARGES IN THERMALLY OXIDIZED (100), (110), (111), and (511) SILICON | |
| 12. PERSONAL AUTHOR(S)<br>Susan C. Vitkavage and Eugene A. Irene | |
| 13a. TYPE OF REPORT<br>Interim Technical<br>13b. TIME COVERED<br>FROM _____ TO _____ | 14. DATE OF REPORT (Yr., Mo., Day)<br>December 6, 1990<br>15. PAGE COUNT<br>42 |
| 16. SUPPLEMENTARY NOTATION<br>Journal of Applied Physics | |
| 17. COSATI CODES<br>FIELD / GROUP / SUB. GR. | 18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number) |

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Trends in the electronic properties of the Si-$SiO_2$ interface with various processing have been frequently reported. The present study focuses on silicon substrate orientation dependent trends in fixed oxide charge, $Q_f$, and interface trap charge, $D_{it}$, for four silicon orientations: (100), (110), (111), and (511), for oxidation temperatures in the 750-1100°C range, with and without hydrogen-containing post-metal anneals, and for processing within and without a cleanroom. It is found that the presence of mobile ionic charge in non-cleanroom processing and the lack of post-metal annealing can either obscure or enhance some trends. Both $Q_f$ and $D_{it}$ increase for decreasing oxidation temperature for all silicon orientations. The orientational ordering of the charges varies with oxidation temperature and is dominated by the silicon atom areal density at the lowest temperatures with (110) Si having the highest charge, but a change to the (111) orientation is observed at higher oxidation temperatures. This orientational charge parallels the orientational oxidation rate ordering but not the intrinsic stress. A model is proposed that considers the orientationally dominated oxidation rate, viscous relaxation, and strain accomodation across the interface as crucial processes.

| | |
|---|---|
| 20. DISTRIBUTION/AVAILABILITY OF ABSTRACT<br>UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐ | 21. ABSTRACT SECURITY CLASSIFICATION<br>Unclassified |
| 22a. NAME OF RESPONSIBLE INDIVIDUAL<br>Dr. David L. Nelson | 22b TELEPHONE NUMBER (Include Area Code)<br>(202) 696-4410<br>22c. OFFICE SYMBOL |

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE

SECURITY CLASSIFICATION OF THIS PAGE

# An Investigation of Si–$SiO_2$ Interface Charges in Thermally Oxidized (100), (110), (111), and (511) Silicon

Susan C. Vitkavage and Eugene A. Irene
Department of Chemistry, University of North Carolina. Chapel Hill,
Chapel Hill, North Carolina 27599-3290.

Hisham Z. Massoud
Department of Electrical Engineering, Duke University,
Durham, North Carolina 27706.

*ABSTRACT*

Trends in the electronic properties of the Si–$SiO_2$ interface with various processing have been frequently reported. The present study focuses on silicon substrate orientation dependent trends in fixed oxide charge, $Q_f$, and interface trap charge, $D_{it}$, for four silicon orientations: (100), (110), (111), and (511), for oxidation temperatures in the 750–1100°C range, with and without hydrogen-containing post-metal anneals, and for processing within and without a cleanroom. It is found that the presence of mobile ionic charge in non-cleanroom processing and the lack of post-metal annealing can either obscure or enhance some trends. Both $Q_f$ and $D_{it}$ increase for decreasing oxidation temperature for all silicon orientations. The orientational ordering of the charges varies with oxidation temperature and is dominated by the silicon atom areal density at the lowest temperatures with (110) Si having the highest charge, but a change to the (111) orientation is observed at higher oxidation temperatures. This orientational charge ordering parallels the orientational oxidation rate ordering but not the intrinsic stress. A model is proposed that considers the orientationally dominated oxidation rate, viscous relaxation, and strain accommodation across the interface as crucial processes.

## *INTRODUCTION*

The control of charges at the Si–$SiO_2$ interface is of crucial importance for the fabrication of small-geometry devices. Thus, the relationship between the chemical and physical nature of the interfacial region and the dependence on various processing parameters has been the focus of much investigation. Early studies reported that the silicon surface could be electronically stabilized by a thermally grown oxide.[1] More recently, it was suggested that successful device fabrication was dependent upon the control of four types of charges that occur in thermally oxidized silicon, namely the interface trap charge ($Q_{it}$), the fixed oxide charge ($Q_f$), the mobile ionic charge ($Q_m$), and the oxide trapped charge ($Q_{ot}$).[2] In particular, most studies have focused on the two types of electrical charge that are closely related to the interfacial region, namely the interface trap charge and the oxide fixed charge. The interface trap charge is the charge on interface traps, also called surface states.

Both the fixed oxide charge and interface trap charge display strong dependencies on oxidation processing variables. In particular, $Q_f$ depends on whether the oxidation ambient is dry oxygen or steam,[3–5] the oxidation temperature with higher temperatures resulting in lower charge densities,[3–7] and on the orientation of the silicon substrate with the (111) orientation having a higher $Q_f$ value than (100).[3,5–8] In addition, $Q_f$ can be reduced by high temperature annealing in such inert ambients as nitrogen, argon, or helium.[3–11]

There exist some discrepancies in the literature regarding the dependencies of the interface trap charge $Q_{it}$. Usually reported as the interface trap density distribution $D_{it}$ ($cm^{-2}/eV$), it displays the same orientation dependence as does $Q_f$. However, conflicting data exists on the effect of oxidation temperature[4–6,13–15] and high-temperature annealing[4–6,10,13–16] on $Q_{it}$. Though high-temperature annealing of interface traps is less well characterized, substantial data exists that shows a minimization of $Q_{it}$ by low-temperature annealing in a hydrogen-containing ambient.[5,15–17].

Since fixed oxide charge and interface trap charge often display the same process dependencies, it is tempting to speculate that these charges have a similar origin. Recent

oxidation studies have shown a possible relationship between the oxidation temperature and many oxide properties as is illustrated schematically in Fig. 1.[18] It is seen that $Q_f$ and $D_{it}$ as well as the $SiO_2$ film properties of intrinsic stress, density and refractive index all increase with decreasing oxidation temperature and all anneal to lower values. Though speculation is tempting, the exact chemical and physical origin of these is still unknown. It should be noted that $Q_f$ and $D_{it}$ are usually measured after one or several processing steps, which must include oxidation or deposition of a dielectric. Hence, the measured $D_{it}$ is a sum of initial number of states or charges associated with the silicon surface plus any changes due to processing. Therefore, if we assume in a first-order model that the initial number of states for a bare silicon surface, $D_{it}(I)$, is proportional to the silicon surface atom density, hence constant, any changes in the measured $D_{it}$ are wholly contained in the processing term, $D_{it}(P)$, which may be positive or negative. The measured $D_{it}$ can be expressed as

$$D_{it} = D_{it}(I) + D_{it}(P) , \tag{1}$$

and similarly for $Q_f$. The processing terms for thermally grown $SiO_2$ films contain the influence of temperature, ambient, rate, impurities and substrate orientation.

The purpose of this study is to attempt to separate the processing effects of temperature, oxidation rate, substrate orientation, and cleanliness. The implications of film stress, post-metal annealing, and sodium contamination on $Q_f$ and $D_{it}$ are directly addressed. The observed trends in $Q_f$ and $D_{it}$ will be compared and discussed in the light of current models and recent observations. A complex picture emerges, but important parameters are identified. Much of the data reported herein is new as four different orientations of silicon were processed simultaneously, but there is some overlap with previous studies with appropriate comparisons. Since controversies exist in this area, we believe that overlaping systematic studies and comparisons with similar studies are useful. This is particularly important, since we show the effects of processing cleanliness on the trends in the electrical data.

## *EXPERIMENTAL PROCEDURES*

Two independent sets of metal-oxide-semiconductor (MOS) structures were prepared on single-crystal silicon substrates under similar processing conditions, in order to determine the effect of mobile-ion contamination, most likely Na ions, on the observed trends in $Q_f$ and $Q_{it}$. The first set of samples was prepared in the non-cleanroom facility of the University of North Carolina. The second set was prepared in the cleanroom facilities of Duke University and the Microelectronics Center of North Carolina (MCNC). The results from these two sets of samples will be referred to hereafter as the *cleanroom* and *non-cleanroom* results.

Processing steps for the non-clearoom samples:

Lightly boron-doped p-type silicon (100), (110), and (111) wafers with resistivities in the 2–5 Ω-cm range were used in the non-clearoom study.The samples were cleaned using a modification of the RCA method,[19], which consists of mixtures of $NH_4OH$:$H_2O_2$:$H_2O$ and HCl:$H_2O_2$:$H_2O$ with both in the respective portions of 1:1:5, followed by a 10-sec concentrated HF dip with each step separated by thorough deionized (DI) water rinses and finally a clean-$N_2$ blow dry.

The wafers were loaded into a double-walled fused-silica tube of the oxidation furnace in an inert $N_2$ ambient, oxidized for a specified time, and pulled fast into the endcap in the oxidizing ambient with a pull time shorter than 5 sec. Some wafers received a post-oxidation anneal (POA) in $N_2$ at the oxidation temperature. Dry oxygen of 99.99% purity, containing less than 6 ppm of water as measured at the exit of the oxidation tube, was used as the oxidizing ambient.

The wafers were oxidized at five temperatures in the 750°C–1100°C range, with the resulting oxide thicknesses varying from 25 nm on (100) wafers oxidized at 750°C to 90 nm on (110) wafers oxidized at 1100°C. Oxide thicknesses were measured with a high-precision manual ellipsometer.

Aluminum dots 0.6 $\mu$m-thick were evaporated on the oxidized wafers in vacuum using a resistively heated source. Some of the wafers then received a 30 min post-metallization anneal (PMA) at 400°C in forming gas (FG), consisting of 10% $H_2$ and 90% $N_2$ at 400°C. Samples with and without PMA will be hereafter referred to as PMA and NPMA samples, respectively.

Processing steps for the cleanroom samples:

Oxidations of p-type (100), (110), (111), and (511) silicon wafers with resistivities in the 2-20 $\Omega$-cm range were performed in the cleanroom facilities at Duke University. All wafers were cleaned using the modified RCA cleaning sequences prior to oxidation.[19] The wafers were oxidized at the temperatures and for the times indicated in Table I. All samples were pulled fast into the endcap in the oxidizing ambient. Upon cooling, the wafers were stored in a dry box continuously purged with pure nitrogen until all oxidations were completed.

A blanket layer of aluminum was evaporated on the oxidized wafers using a resistively heated evaporator located in the class-1 cleanroom facility at MCNC. The (100), (111), and (511) 4-inch diameter wafers from all oxidations were metallized together, and the (110) 3-inch diameter wafers were metallized in a separate run. Capacitors with guard-ring sturctures were defined using lithography, and a second blanket layer of Al was evaporated on the backside of the wafers after the backside oxide had been etched for backside contact.

Upon completion of the metallization steps, the wafers were cleaved in half, with one half of each wafer receiving a 30 min PMA at 400°C in FG, and the other half receiving no anneal (NPMA).

## *DATA ANALYSIS*

The oxide fixed charge density is calculated from the relationship[22]

$$Q_f = C_{ox} ( \phi_{ms} - V_{FB} ) , \qquad (2)$$

where $C_{ox}$ is the oxide capacitance per unit area, $V_{FB}$ the measured flatband voltage, and $\phi_{ms}$ the metal-semiconductor work-function difference. The oxide fixed charge density $Q_f$

is usually obtained from high-frequency (1 MHz) capacitance-voltage made on MOS structures that received a post-metallization anneal. This ensures minimum flatband-voltage variations due to interface traps.[5] In this study, we will also report $Q_f$ measurements from NPMA samples. Measurements of $Q_f$ on NPMA samples also include the portion of $Q_{it}$ that responds to the high-frequency measurement. For high concentrations of interface traps, this component is expected to be significant. While this charge reporting procedure could be misleading, we include the results in order to explore the contention that incomplete or ineffective PMA can confuse results and obscure or create artificial trends.

Interface trap density $D_{it}$ was obtained combining the high-frequency capacitance-voltage measurements with quasi-static capacitance-voltage measurements using a voltage ramp rate of less than 100 mV/sec. The interface trap density is given by

$$D_{it} = \frac{1}{q\,A}\left[\frac{C_{LF}}{(C_{ox} - C_{LF})} - \frac{C_{HF}}{(C_{ox} - C_{HF})}\right], \tag{3}$$

where $C_{LF}$ and $C_{HF}$ are the low-frequency (or quasi-static) and high-frequency capacitances at a given voltage, respectively, $C_{ox}$ the oxide capacitance per unit area, $A$ the area of the electrode, and $q$ the elementary charge. The high-frequency C-V curve was corrected for the presence of a series resistance by measuring the capacitance and the equivalent parallel conductance in strong accumulation from a conductance-voltage measurement.[20] All data acquisition and analysis were computer-assisted. The surface potential was obtained by numerical integration of the low-frequency C-V curve.[21] All of the measurements of fixed oxide charge and interface trap charge reported in this study were the average of eight or more measurements as obtained from four measurements per sample, with two samples of each orientation prepared for each oxidation, and the results are shown in Table II. The standard deviation of $Q_f$ and $D_{it}$ for the cleanroom samples was less than 5% across each wafer, and the two samples processed identically agreed to within 10% of each other. The non-clearoom (111) and (110) samples showed greater deviations of 15% across a single wafer and 20–30% between two wafers processed identically. However, the non-cleanroom (100) samples displayed even greater deviations of up to 100% across a

wafer. These results are considered unacceptable and will not be reported. The ± values reported in Tables III and IV are the maximum spread of the data.

## *EXPERIMENTAL RESULTS*

*Mobile-Ion Contamination.* It will be demonstrated here that the presence of mobile ionic charges can alter the observation of trends in other charges. Bias-temperature stress high-frequency C-V measurements[20] on the non-cleanroom samples yielded flatband voltage shifts due to mobile-ion contamination $Q_m$ that ranged from - 0.25 V to - 1.0 V, which corresponds to positive $Q_m$ values ranging from 1 to 5 × $10^{11}$ $cm^{-2}$, respectively, and cleanroom samples had flatband voltage shifts of less than - 0.04 V which corresponds to a positive value of $Q_m$ of about 1.5 × $10^{10}$ $cm^{-2}$ for both the 3-inch and 4-inch wafers. An additional limitation imposed by the non-cleanroom evaporator is that a maximum of only four samples could be prepared simultaneously. Therefore, when preparing a large matrix of samples such as used in this study, there may be significant differences in $Q_m$ between samples oxidized together but metallized at different times.

Table II contains a sampling of $Q_f$ and $D_{it}$ data for PMA samples. Cleanroom samples generally have lower $Q_f$ and $D_{it}$ values by factor as large as 4× when compared with non-cleanroom samples. Also the variations with oxidation temperature are more pronounced and the spread in the data is larger for non-cleanroom samples. With the larger absolute values of charges arising from ionic contamination, and the larger variations from sample to sample and on single samples, possible trends in the data from process variations may be different. An illustration of this is that no trend is observed in $Q_f$ with oxidation temperature for (100) cleanroom samples, but a clear trend is seen for the corresponding non-cleanroom samples for all orientations. Also a minimum is seen in $D_{it}$ for non-cleanroom samples grown at 900°C but that trend cannot be unambiguously seen for the cleanroom samples. It is therefore crucial to report $Q_m$ values as well as the other charge levels since it is clear that complex cooperative effects occur. Other cleanliness effects are reported below.

*Effects of Low-Temperature Hydrogen Annealing.* Post-metallization annealing (PMA) at 400°C for 30 min in forming gas (FG) profoundly affects the shape of the C-V curves as is most evident in the depletion region which indicates the presence of interface traps.[20] With PMA, there is good agreement between the high- and low-frequency C-V curves in the depletion region, and a corresponding lower interface trap density.

The distribution of interface trap densities as a function of energy in the bandgap indicated that the midgap $D_{it}$ has been reduced by an order of magnitude on the PMA sample. Additionally, the well reported peak[5,15,23] in the interface trap density distribution at about 0.3 eV above the valence band edge for NPMA samples usually observed for damaged Si surfaces is no longer present in the (100) samples and considerably reduced in the (111) samples in the interface trap density distribution of PMA samples. This peak was found on all samples of different orientations that were rapidly removed from the oxidation furnace and cooled in the oxidizing ambient. No other distinct peaks were observed in our samples. Electron-spin resonance studies (ESR)[23] have related this peak to the $P_b$ center which is a trivalent silicon defect or dangling bond. Thus, hydrogen effectively reduces this state on all orientations studied as well as reducing the concentration of all of the silicon bandgap interface traps.

For some NPMA samples, the interface trap densities were so high that a midgap $D_{it}$ was not measurable. These high concentrations of interface traps effectively result in Fermi level pinning thereby rendering part of the silicon gap inaccessible. This was particularly true for (111) samples and occasionally true for (110) samples, which had the highest interface trap densities of the samples studied. For the purpose of comparing orientations, however, the $D_{it}$ data was obtained at potentials in the silicon gap other than at midgap, as noted in the tables. Also from Fig. 2, it is observed that the PMA more dramatically affects the upper part of the silicon bandgap where the deep acceptor traps are located. The upper portion of the bandgap had unmeasurably large concentrations of interface traps - as indicated in the quasi-static C-V curve - prior to PMA which are reduced to below the other levels after PMA. It is interesting to note that for the (111) and (110) orientations, a minimum occurs at about 0.3 eV above the valence band edge for the NPMA samples.

which enables the use of this potential to compare $D_{it}$ levels. By contrast, (100) samples and radiation-damaged silicon show a peak at this surface potential.

*Substrate Orientation and Oxidation Temperature Effects.* Fixed oxide charge for the cleanroom samples is plotted as a function of oxidation temperature for the four substrate orientations in Fig. 3 for PMA and NPMA samples and the data is shown in Table III along with the maximum spread in the data. The ambiguity in $Q_f$ values for the NPMA samples as discussed above should be remembered and thus the usefullness of such data in the interpretation of fundamental phenomena is limited. However, these data are included to investigate the effect of the silicon orientation and oxidation temperature on trends in the charges of samples that have received either no anneals or incomplete anneals, since discrepancies exist in the literature. For all samples and temperatures greater than 750°C, the (111) orientation has the highest fixed oxide charge, with the order in $Q_f$ being

$$Q_f(111) > Q_f(110) \geq Q_f(100) \geq Q_f(511) .$$

At 750°C, there is an apparent change in the ordering, with the (110) orientation having the largest fixed oxide charge. However, while this effect appears to be real and is observed in both PMA and NPMA samples, the maximum spread in the data for NPMA samples precludes an unambiguous interpretation.

Higher oxidation temperatures generally yield lower values of $Q_f$ and while the trend is discernible for PMA samples it is particularly evident for NPMA samples. It is also observed that (110), (511), and (100) PMA samples, oxidized at a temperature higher than 750°C, have approximately the same $Q_f$ value of $1 - 2 \times 10^{11}$ cm$^{-2}$. The largest change between PMA and NPMA samples is seen with the (511) orientation which has a low value of $2 \times 10^{10}$ cm$^{-2}$ at 800°C. Oxide fixed charges on NPMA samples are 4× larger and the spread in the data 2× larger than on PMA samples.

Fixed charge density was also obtained for the three orienations processed in non-cleanroom conditions. These results are plotted in Fig. 4 for PMA samples where it can seen that $Q_f$ decreases with increasing temperature more strongly than in wafers processed

under similar conditions in cleanroom conditions. However, the values of non-cleanrrom $Q_f$ are also significantly larger, the non-cleanroom results did not exhibit a crossover with different orientations. For example, $Q_f$ at 750°C is 3× larger for the non-cleanroom (111) orientation than on cleanroom samples, and 6× larger on the (100) orientation. Similar results are found for NPMA non-cleanroom samples but with both larger values and greater deviations.

Interface trap charge density ($D_{it}$) displays an orientation dependence similar to that of $Q_f$, as is shown in Fig. 5 for PMA and NPMA samples, and that data with maximum spreads is listed in Table IV. For temperatures above 750°C, the orientational ordering is clearly

$$Q_f(111) > Q_f(110) > Q_f(100) \geq Q_f(511) .$$

with NPMA samples having $D_{it}$ an order of magnitude higher than on PMA samples. As discussed above for $Q_f$, for both the NPMA and PMA samples grown at 750°C, there is an apparent change in the ordering of $D_{it}$, with the (110) orientation having the highest interface trap charge density. However, if we consider that for (110), $D_{it}$ is $16 \pm 1 \times 10^{10}$ $cm^{-2}eV^{-1}$ at midgap and for (111) it is $13 \pm 0.6 \times 10^{10}$ $cm^{-2}eV^{-1}$, the maximum deviations make the values nearly the same within 10%. Without post-metallization annealing, $D_{it}$ values for the (111) and (110) orientations were too large to be determined at midgap. However, near a surface potential of 0.3 eV there was no crossover until the oxidation temperature was 1000°C, but here again the maximum error limits in the data render conclusions about the crossover tenuous. There was no crossover in $D_{it}$ for the non-cleanroom samples. Thus, there is a definite orientation dependence for both $Q_f$ and $D_{it}$. However, whether the (111) or (110) orientation exhibits the larger $D_{it}$ is a function of processing, and for NPMA samples, the (110) orientation has a higher $D_{it}$ but the (111) orientation has a higher $Q_f$. It is shown that impurities and annealing greatly alter both the magnitude and orientational dependence of both fixed oxide and interface trap charges.

The temperature dependence of interface trap charges on cleanroom samples is also shown in Fig. 5. These are all midgap values and, as stated above, midgap values were

not always measurable on NPMA samples. This explains why the much higher values of midgap $D_{it}$ on (111) samples are not included in Fig. 5. All samples show an overall decreasing $D_{it}$ with increasing oxidation temperature. However, the magnitude of the decrease depends on both the substrate orientation and the treatment. The midgap $D_{it}$ on the (100) and (110) orientations of PMA samples decrease more sharply with increasing oxidation temperature than on the other orientations. The midgap $D_{it}$ at 1000°C is 2.5 and 2.0 times smaller than those on samples oxidized at 750°C for the (100) and (110) orientations, respectively. The midgap $D_{it}$ on the (511) samples shows only a slight decrease at the higher oxidation temperatures, and the (111) orientation shows little temperature dependence within experimental error. If the displayed temperature dependence is also considered to be dependent on the substrate orientation, then we find that the change in $D_{it}$ with temperature ($\Delta D_{it}$) over the temperature range in this study follows the order

$$\Delta D_{it}(100) \geq \Delta D_{it}(110) > \Delta D_{it}(511) > \Delta D_{it}(111) .$$

There is a stronger temperature dependence of $D_{it}$ on NPMA samples, with $D_{it}$ at 1000°C being three times smaller than that at 750°C for the (100) and (511) orientations.

This orientation-dependent temperature behavior was also observed in the non-cleanroom experiment, where an even larger temperature range was investigated. The interface trap density at 0.3 eV for (111), and at midgap for the (110) orientation of NPMA samples is plotted in Fig. 6. The interface trap density for the (111) orientation is fairly constant over this temperature range. Again, the non-cleanroom values are higher than the cleanroom values by approximately a factor of two.

Similar observations have already been reported. Razouk and Deal[5] reported a temperature dependence of interface traps in the 900°C–1200°C range for NPMA cleanroom samples prepared in a manner almost identical to that used in this study. From their data,[5] the slope of the interface trap density as a function of temperature for the (100) and (111) orientations was calculated, and the results are compared with the results of this study in Table V. The (100) orientation displays a stronger temperature dependence by nearly an order of magnitude, and good agreement is seen between the results of this study and

those of Razouk and Deal.[5] As the oxides studied by Razouk and Deal were much thicker than those investigated in this study, a quantitative comparison of $D_{it}$ values with this study could only be done for the 8-hour 1000°C oxidation. As-oxidized midgap interface trap density reported by Razouk and Deal[5] at 1000°C were $2.5 \times 10^{12}$ $cm^{-2}$ and $9.0 \times 10^{10}$ $cm^{-2}$ for the (111) and (100) orientations, respectively. The corresponding values obtained in this study were $2.2 \times 10^{12}$ $cm^{-2}$ and $1.7 \times 10^{11}$ $cm^{-2}$ for the (111) and (100) orientations, respectively.

*Oxidation Rate Effects.* In order to investigate the influence of the oxidation rate on $Q_f$ and $D_{it}$, several experiments were carried out on $SiO_2$ films grown at 1000°C. This temperature was selected to minimize any effects that might arise due to the presence of intrinsic stress at the interface which is known to be smaller at higher oxidation temperatures.[24,25] The thickness of the oxides in this experiment varied from 500–640Å for the 1-hour oxidation to 2050–2400Å for the 8-hour oxidation for the (100) and (111) orientations, respectively.

The dependence of fixed oxide charge results on oxidation time at 1000°C is plotted in Fig. 7 for PMA samples with the data listed in Table VI. For all but the (110) orientation, a slight decrease in $Q_f$ is observed for longer oxidation times, i.e. for slower oxidation rates and thicker oxides. The results are similar for NPMA samples, whose data is listed in Table VI, but with approximately 2× larger charges. An increase in $Q_f$ for thinner oxides has also been reported.[11]

The dependence of interface trap charges of PMA samples on oxidation time at 1000°C is plotted in Fig. 8 with the data listed in Table VII. A more discernible decrease in interface trap charge with increasing oxidation time and decreasing oxidation rate is ovserved. Hung and Cheng[15] have reported a similar dependence of $D_{it}$ for oxide thicknesses less than 500Å, and their etch-back experiment confirmed that the observed thickness dependence was due to the oxidation process, and not due to any subsequent steps. Here again, the results are similar for NPMA samples, whose data is listed in Table VII, but with a 10× larger charge density and a smaller change with oxidation time.

The dependence of the overall $SiO_2$ growth rate on oxidation temperature for the four orientations is shown in Fig. 9. The overall oxidation rate was obtained by dividing the final oxide thickness by the total oxidation time. A crossover between the oxidation rates on the (110) and (111) orientations is seen at 750°C. Such a rate crossover has been previously reported,[26–28] and studied in detail. Figures 3 and 5, showing the dependence of $Q_f$ and $D_{it}$ on oxidation temperature, display evidence for crossover or at least for the convergence of the charge levels with oxidation temperature. It should be noted that the overall oxidation rate is different from the oxidation rate at the end of the oxidation before the sample is removed from the furnace. In this study, the oxidation time at 750°C is past the reported interfacial oxidation-rate crossover point.[26–28] Therefore, the final interfacial oxidation rate ordering is actually (111)>(110). The overall thicknesses of the oxides do not yet reflect this change, as the (111) must catch up with (110), i.e. the thickness crossover lags the rate crossover.[26–28] The non-cleanroom samples were oxidized one hour longer than the cleanroom samples, and the change in interfacial oxidation rate is evident in the overall growth rate, i.e. the thickness of the oxides on the (111) orientation samples was larger than that on (110) samples after the additional hour. The non-cleanroom results did not show the same crossover in $D_{it}$ and $Q_f$, with the (111) orientation always showing greater charge levels, but when one considers the actual oxidation rate at the interface, this is not necessarily inconsistent with the above results. Thus, the data strongly suggest that the charges scale with the fastest oxidizing surface.

For charges that exist at the Si–$SiO_2$ interface and possibly scale with the $SiO_2$ growth, a correlation should be attempted with the interfacial oxidation rate and not the overall oxidation rate. It is also possible that the differences in $D_{it}$ at 750°C for the cleanroom samples are not statistically significant, with $D_{it}$ of $1.55 \times 10^{11}$ $cm^{-2}$ and $1.34 \times 10^{11}$ $cm^{-2}$ on (110) and (111), respectively. However, the difference in $Q_f$ is significant, with values of $1.1 \times 10^{12}$ $cm^{-2}$ and $5.9 \times 10^{11}$ $cm^{-2}$ on (110) and (111), respectively. This can be understood by considering the oxidation rate at the interface. Initially, the (110) orientation is oxidizing the fastest. We have shown that the substrate orientation is important in determining the ordering of $Q_f$ and $D_{it}$ which are both the highest on (110). Since new oxide is always

being formed at the interface, any change in oxidation rate ordering - and consequently the orientational ordering of $Q_f$ and $D_{it}$- will first be evident at the interface and in the interface trap charge. The fixed oxide charge, on the other hand, is thought to be displaced by about 50Å from the interface,[22] and the change will not be detected until those 50Å have replaced by the new oxide. It appears that a slow interfacial oxidation rate at a constant oxidation temperature yields low values of $Q_f$ and $D_{it}$ for otherwise similar sample preparation procedures. While this is not yet fully understood, it is useful processing information. One need simply follow a rapid oxidation or other film formation procedure by a slower thermal oxidation which will effectively decrease the interfacial charges to acceptable levels. It is also well known that a zero oxidation rate or an anneal in an inert ambient decreases both $Q_f$ and $D_{it}$ values.[7] However, we have no reason to believe that this anneal effect is the same as the low oxidation-rate effect.

## *DISCUSSION*

*Silicon Surface Orientation.* The observed dependence of the interface traps and fixed oxide charges on the silicon substrate orientation can be compared with the density of silicon surface atoms ($C_{Si}$) which is known to follow the order[27]

$$C_{Si}(110) > C_{Si}(111) > C_{Si}(511) > C_{Si}(100) .$$

The (511) orientation is of particular interest because recent diffraction studies have identified the (511) plane as a vicinal surface consisting of (100) steps and (111) risers.[29] It has been establised that the silicon oxidation rate in the initial oxidation regime of oxides up to 300Å follows the order of $C_{Si}$ over the 600°C–1000°C temperature range.[27,28] For larger thicknesses, a crossover is observed with the (111) orientation yielding a higher oxidation rate than the (110) orientation. In the present study with 500Å-thick oxide films, the oxidation regime was above the crossover to where the (111) orientation is the fastest. The observed $D_{it}$ and $Q_f$ values track with the oxidation rates rather than the silicon atom areal density with the (111) yielding both the higher charge levels and interfacial oxidation rate. Near the lowest temperature investigated of 750°C, $D_{it}$ values on the (111) and (110)

orientations become nearly equal with a possibility of a crossover. This suggests that at lower temperatures, the dominance of $C_{Si}$ is regained. Additional studies using very thin oxides grown at even lower temperatures will be required to further elucidate this issue.

A quantitative comparison of $D_{it}$ to the surface atom density is made by comparing the ratio of surface atom densities for the same two orientations. This correlation is shown in Table VIII for the data at 750°C, with the quantitative agreement being quite good but diverging above 750°C for all orientations. This gives credence to the idea that at lower oxidation temperatures, the silicon atom density is important. It is noted that $Q_f$ and $D_{it}$ for the (511) orientation displayed no clear distinction from the (100) orientation, with values both greater than and smaller than $Q_f$ and $D_{it}$ on the (100) orientation. There was considerably greater variation in the measured values on (511), possibly owing to the more complex vicinal nature of the orientation.[29] It should also be noted that the orientation and oxidation temperature effects are somewhat obscured both by PMA in hydrogen-containing ambients and the lack of cleanroom conditions. Hydrogen atoms bonded to the silicon surface reduce all charges while other impurities usually tend to increase them. The result is that the strictly silicon-orientation-dictated amounts of charges are altered and perhaps masked by the influence of hydrogen and/or impurities on the charges. It has often been reported that chemical-vapor-deposited oxide (CVD $SiO_2$) films exhibit higher $Q_f$ and $D_{it}$ levels than thermally oxidized silicon. However, recently published studies show that with the use of very low deposition rates along with careful control of other processing variables and cleanroom conditions, the charge levels for CVD oxides can approach those of thermally oxidized silicon, suggesting that the improved registration obtainable with slower deposition rates across the substrate–film interface is important.[30,31] Furthermore, $SiO_2$ grown at 1100°C on (100) silicon with PMA show decidedly smaller $Q_f$ as the partial pressure of oxygen is decreased.[32] The decrease in oxygen reduces the oxidation rate at the same oxidation temperature.

*Intrinsic Stress.* Intrinsic $SiO_2$ stress ($\sigma_i$) which arises from the molar volume change

from Si to $SiO_2$ has been observed to follow the silicon substrate orientation order as[25,33-35]

$$\sigma_i(110) > \sigma_i(511) \geq \sigma_i(100) > \sigma_i(111) .$$

As the oxide growth strain which is caused by the molar volume change during oxidation is thought to be the same regarless of the silicon orientation, the ordering for the resulting $\sigma_i$ was predicted to follow Young's modulus. This would lead to the (111) orientation as having the highest stress value.[28] This prediction was not borne out in experiment and several similar models have proposed that if oxidation occurs laterally at surface steps then a smaller stress would result.[36,37] It has been shown that the (111) orientation of silicon has a step density nearly twice that on the (100) orientation,[38] and a detailed mechanism has been proposed for the production and oxidation of steps on a silicon surface.[37] For all silicon orientations, $\sigma_i$ decreases with increasing oxidation temperature and after high-temperature annealing.[24,25,39,40]

With the exception of the (111) orientation, both $Q_f$ and $D_{it}$ follow the intrinsic stress related orientation and oxidation temperature dependence. It should be noted that the thermal expansion component of the total stress ($\sigma_{th}$) develops upon cooling from the oxidation temperature and has the opposite temperature dependence of both $\sigma_i$ and the charges.[25] The anomalously low $\sigma_i$ observed for the (111) orientation was attributed to lateral oxidation at steps or at rough surface regions, and may also be the cause for the highest charge level found on this orientation. Roughness is known to increase both interface traps and charges.[38]

The present experimental results combined with published studies show that no single process paramater determines the variation of the interface charges. However, based on the experimental results now available, it is reasonable to propose that the measured values of $Q_f$ and $D_{it}$ can derive from the two primary sources. First, on the oxidized silicon surface, an initial charge level arises from the registry of the silicon surface with the oxide. At the interface, the large change in volume causes a misregistry of bonds with commensurate intrinsic stress leading to orientational and stress sensitive interface charges. It is then easy to imagine how the oxidation rate, the oxidation temperature, the oxygen partial

pressure, the silicon orientation, and the specific geometry across the interface can affect the registry and hence the charges. Second, there is a relaxation component that can reduce the misregistry and thereby lower the interfacial charge. Higher oxidation temperatures (reduced stress), reduced oxidation rate (stress relaxation and registry) and annealing are the primary relaxation procedures. Annealing (temperature and time) enhances the attainment of optimum registry, and annealing with hydrogen atoms can further reduce interface charges through hydrogen-bond formation at sites that for geometrical (steric) reasons cannot attain full bond registry across the interface.

## *SUMMARY*

1. The effects of cleanliness on interface charges and traps were measured using $Q_m$, and it was found that both $Q_f$ and $D_{it}$ increased with an increase in $Q_m$. This observed trend can be both enhanced or obscured with high $Q_m$ levels. This factor along with different anneals may explain why different trends were reported in the literature for the processing effects on charges.

2. Strong orientation effects are observed for both $Q_f$ and $D_{it}$ with the (111) orientation displaying the highest charge levels at all but the lowest oxidation temperature in this study where the (110) orientation dominates. This change in ordering strongly suggests that at higher oxidation temperatures, factors other than the silicon surface atom density is important for controlling charges.

3. Both $Q_f$ and $D_{it}$ decrease with higher oxidation temperatures. Intrinsic stress also decreases with increasing oxidation temperature and at first a direct correlation seems to exist between charge and stress. However, the (111) orientation has the largest charge at oxiation temperatures higher than 750°C and the lowest intrinsic stress. The anomalously low stress for the (111) orientation was attributed to surface steps or roughness. Perhaps this also causes the higher charge levels.

4. A crossover in both oxidation rate and charges leads to the notion of the dependence of charge on interfacial oxidation rate. The specific process steps leading to better interfacial

registry or the attainment of registry seem to provide a working model for predicting the final interfacial charge levels both for thermal oxides in this study and for CVD oxides reported in the literature. Thus, annealing, high oxidation temperatures, and low oxidation rates all reduce charge and stress, while the opposite processing increase charge.

5. Anneals in hydrogen-containing ambients can dominate both $Q_f$ and $D_{it}$ by reducing charge levels by orders of magnitude and leveling both oxidation temperature and silicon surface atom density trends in the charges. The marked effect on deep acceptor states was observed for the (111) and (110) silicon orientations. The notion that hydrogen bonds preferentially to certain energetically different sites may provide an analysis tool for the different sites.

*ACKNOWLEDGEMENTS*

The authors gratefully acknowledge the support of the Semiconductor Research Corporation and the Office of Naval Research, and the Microelectronics Center of North Carolina for providing the facilities used in the cleanroon part of this work.

*REFERENCES*


1. M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, Bell Sys. Tech. J., **38**, 749 (1959).
2. B. E. Deal, J. Electrochem. Soc., **127**, 979 (1980).
3. B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, J. Electrochem. Soc., **114**, 266 (1967).
4. D. J. Breed and R. P. Kramer, Solid-State Electronics, **19**, 897 (1976).
5. R. R. Razouk and B. E. Deal, J. Electrochem. Soc., **126**, 1573 (1979).
6. F. Montillo and P. Balk, J. Electrochem. Soc., **118**, 1463 (1971).
7. A. I. Akinwande, C. P. Ho, and J. D. Plummer, Appl. Phys. Lett. , **45**, 263 (1984).
8. D. R. Lamb and F. R. Badcock, Int. J. of Electronics, **24**, 11 (1968).
9. D. M. Brown and P. V. Gray, J. Electrochem. Soc., **115**, 760 (1968).
10. S. I. Raider, R. A. Gdula, and J. R. Petrak, Appl. Phys. Lett., **27**, 150 (1975).
11. H. P. Vyas, G. D. Kirchner, and S. J. Lee, J. Electrochem. Soc., **129**, 1757 (1982).
12. E. Arnold, J. Ladell, and G. Abowitz, Appl. Phys. Lett., **13**, 413 (1968).
13. E. A. Fogels and C. A. T. Salama, J. Electrochem. Soc., **118**, 2002 (1971).
14. K. Hofmann and M. Schultz, J. Electrochem. Soc., **132**, 2201 (1985).
15. K. K. Hung and Y. C. Cheng, J. Electrochem. Soc., **134**, 2814 (1987).
16. Y. T. Yeow, D. R. Lamb, and S. D. Brotherton, J. Phys. D: Appl. Phys., **8**, 1495 (1975).
17. E. Kooi, Phillips Res. Rep., **20**, 578 (1965).
18. E. A. Irene, Phil. Mag. B, **55**, 131 (1987).
19. W. Kern and D. A. Puotinen, RCA Review, **31**, 187 (1970).
20. E. H. Nicollian and J. R. Brews, *MOS (Metal-Oxide-Semiconductor) Physics and Technology*, John Wiley and Sons, New York, N. Y. (1982).
21. C. N. Berglund, IEEE Trans. Eelctron Dev., **TED-13**, 701 (1966).
22. M. Kuhn, Solid-State Electronics, **13**, 873 (1970).
23. N. M. Johnson, D. K. Biegelsen, and M. D. Moyer, in *Physics of MOS Insulators*, p. 311, S. T. Pantelides, Editor, Pergamon Press, New York, N. Y. (1980).
24. E. Kobeda and E. A. Irene, J. Vac. Sci. Technol., **B5**, 15 (1987).

25. E. Kobeda and E. A. Irene, J. Vac. Sci. Technol., **B4**, 720 (1986).
26. H. Z. Massoud, J. D. Plummer, and E. A. Irene, J. Electrochem. Soc., **132** 1745, 2685, 2693 (1985).
27. E. A. Lewis and E. A. Irene, J. Electrochem. Soc., **134**, 2333 (1987).
28. E. A. Irene, H. Z. Massoud, and E. Tierney, J. Electrochem. Soc., **133**, 1253 (1986).
29. K. Ueda and M. Inoue, Surf. Sci., **161**, L578 (1985).
30. J. Batey and E. Tierney, J. Appl. Phys., **60**, 3136 (1986).
31. S. S. Kim, D. V. Tsu, and G. Luckovsky, J. Vac. Sci. Technol., **A6**, 1740 (1988).
32. S. P. Murarka, Appl. Phys. Lett., **34**, 587 (1979).
33. E. P. EerNisse, Appl. Phys. Lett., **30**, 290 (1977).
34. W. A. Tiller, J. Electrochem. Soc., **127**, 625 (1980).
35. E. A. Irene, E. Tierney, and J. Angilello, J. Electrochem. Soc., **129**, 2594 (1982).
36. L. M. Landsberger and W. A. Tiller, Appl. Phys. Lett., **51**, 1416 (1987).
37. G. Ghibaudo, Phil. Mag. B, **55**, 147 (1987).
38. N. F. Mott, Phil. Mag. B, **55**, 117 (1987).
39. B. Leroy, Phil. Mag. B, **55**, 159 (1987).
40. P. O. Hahn and M. Henzler, J. Vac. Sci. Technol., **A2**, 574 (1984).

## *FIGURE CAPTIONS*

Figure 1. Schematic representation of the effect of oxidation temperature on some oxide property F(T), where F(T) is the refractive index n, the oxide density $\rho$, the intrinsic stress $\sigma_i$, and the interface charges $Q_f$ and $D_{it}$ from Ref. 18.

Figure 2. Interface trap density $D_{it}$ plots for a p-type (111) sample (a) without a post-metallization anneal (NPMA) and (b) with a post-metallization anneal (PMA).

Figure 3. The dependence of fixed oxide charge $Q_f$ on oxidation temperature for the four silicon orientations studied in the cleanroom experiment, (a) with a post-metallization anneal (PMA), and (b) without a post-metallization anneal (NPMA).

Figure 4. The dependence of fixed oxide charge $Q_f$ on oxidation temperature for the three silicon orientations studied in the non-cleanroom experiment including a post-metallization anneal (PMA).

Figure 5. The dependence of interface trap density $D_{it}$ on oxidation temperature for the four silicon orientations studied in the cleanroom experiment, (a) with a post-metallization anneal (PMA), and (b) without a post-metallization anneal (NPMA).

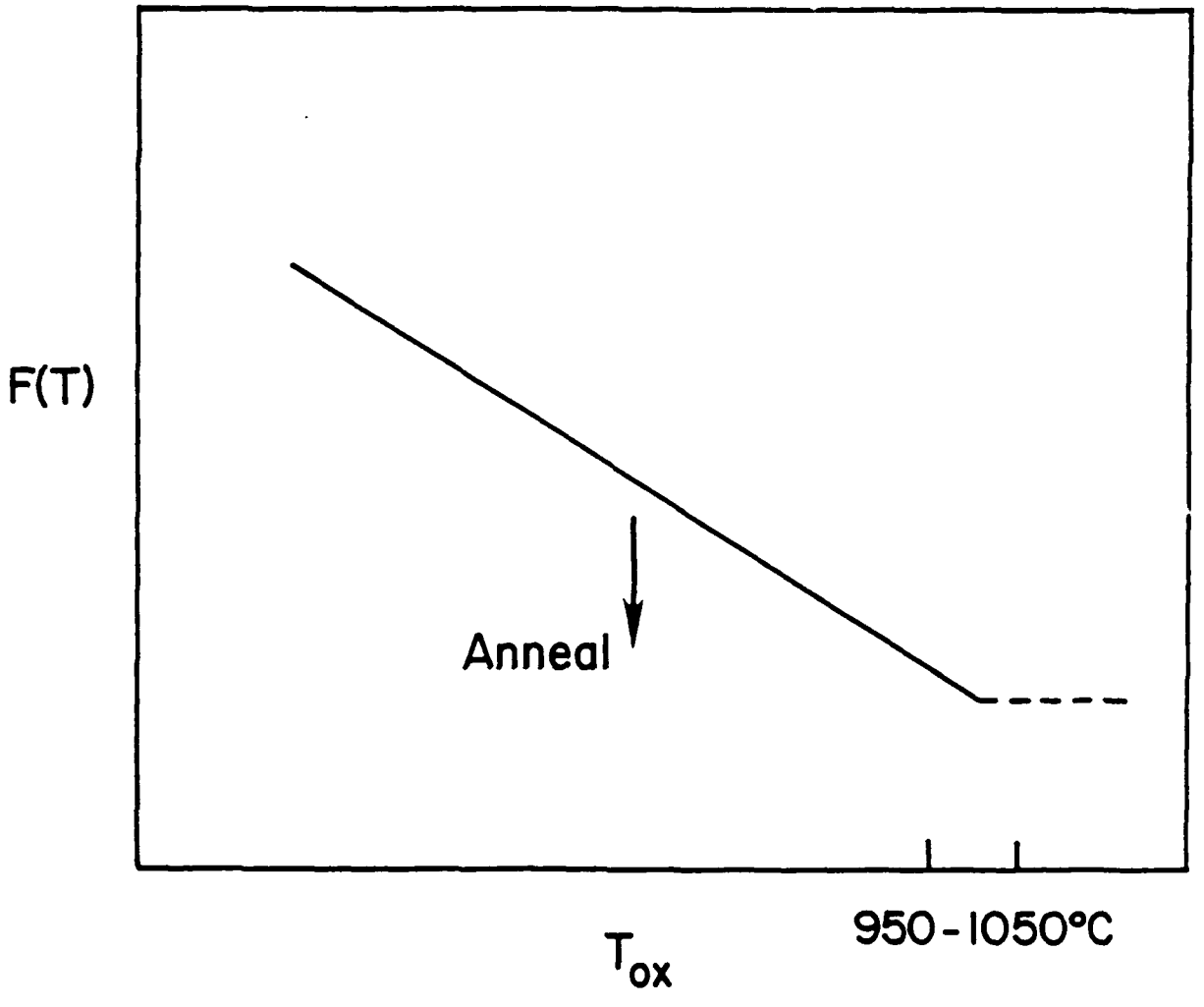
Figure 6. The dependence of interface trap density $D_{it}$ on oxidation temperature for the (111) and (110) silicon orientations studied in the non-cleanroom experiment without a post-metallization anneal (NPMA).

Figure 7. The dependence of oxide fixed charge $Q_f$ on oxidation time for the four silicon orientations studied in the cleanroom experiment including a post-metallization anneal (PMA).

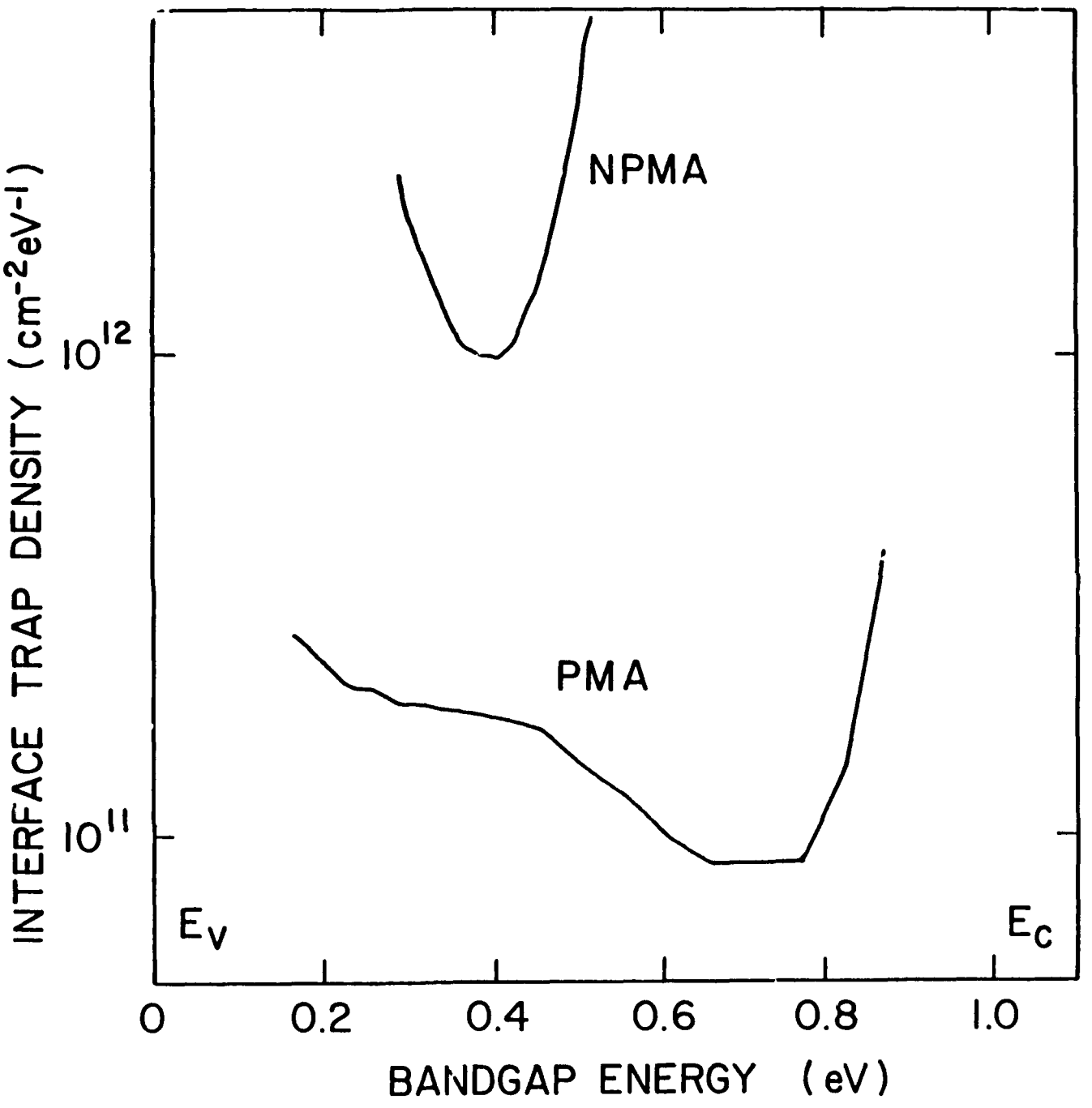
Figure 8. The dependence of interface trap density $D_{it}$ on oxidation time for the four silicon orientations studied in the cleanroom experiment including a post-metallization anneal (PMA).

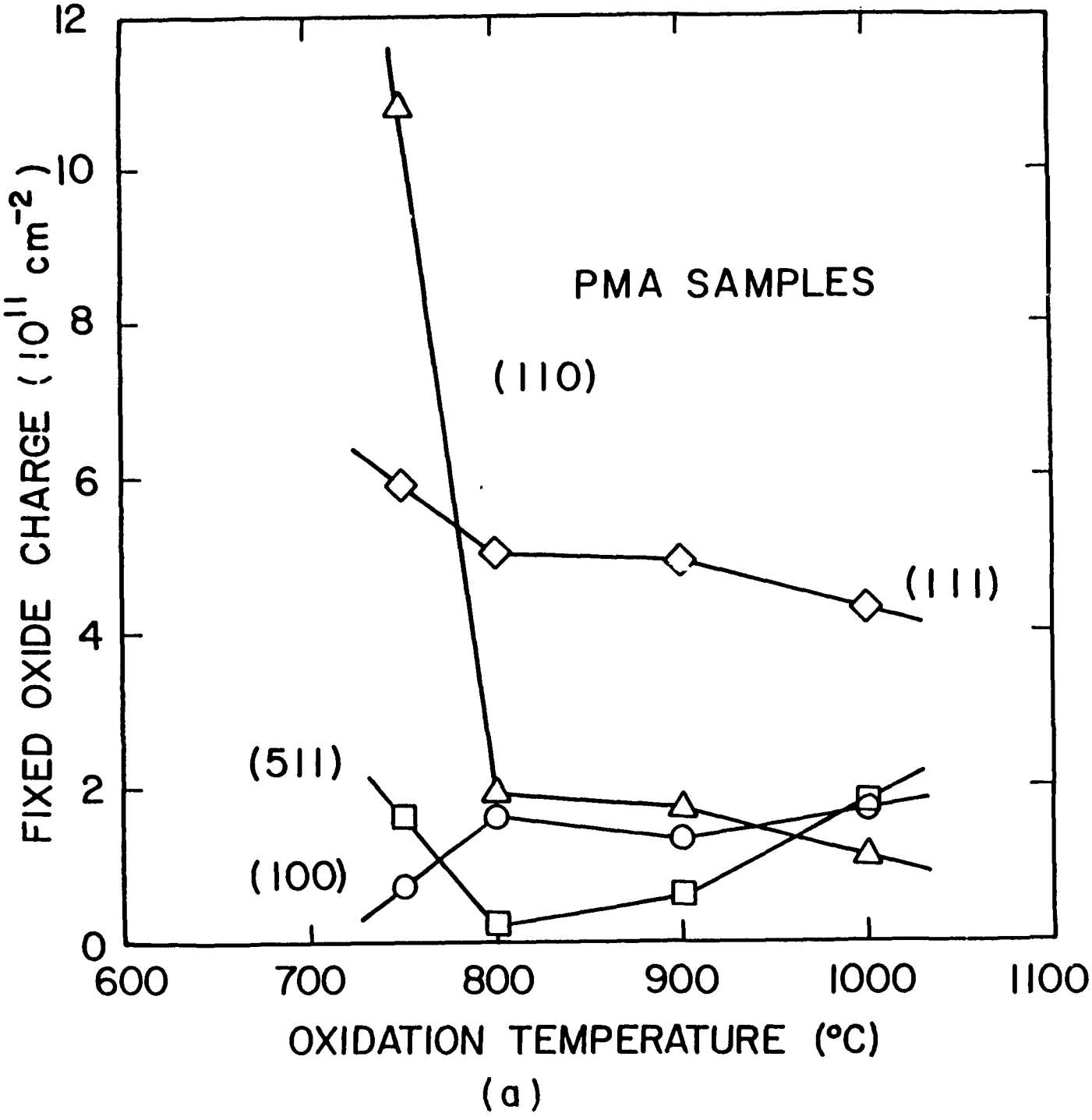
Figure 9. Overall oxiation rate at 750°C and 800°C showing a crossover in the rates of oxidation of the (110) and (111) orientations.

## $SiO_2$ Film Properties, F(T), vs Oxidation Temperature

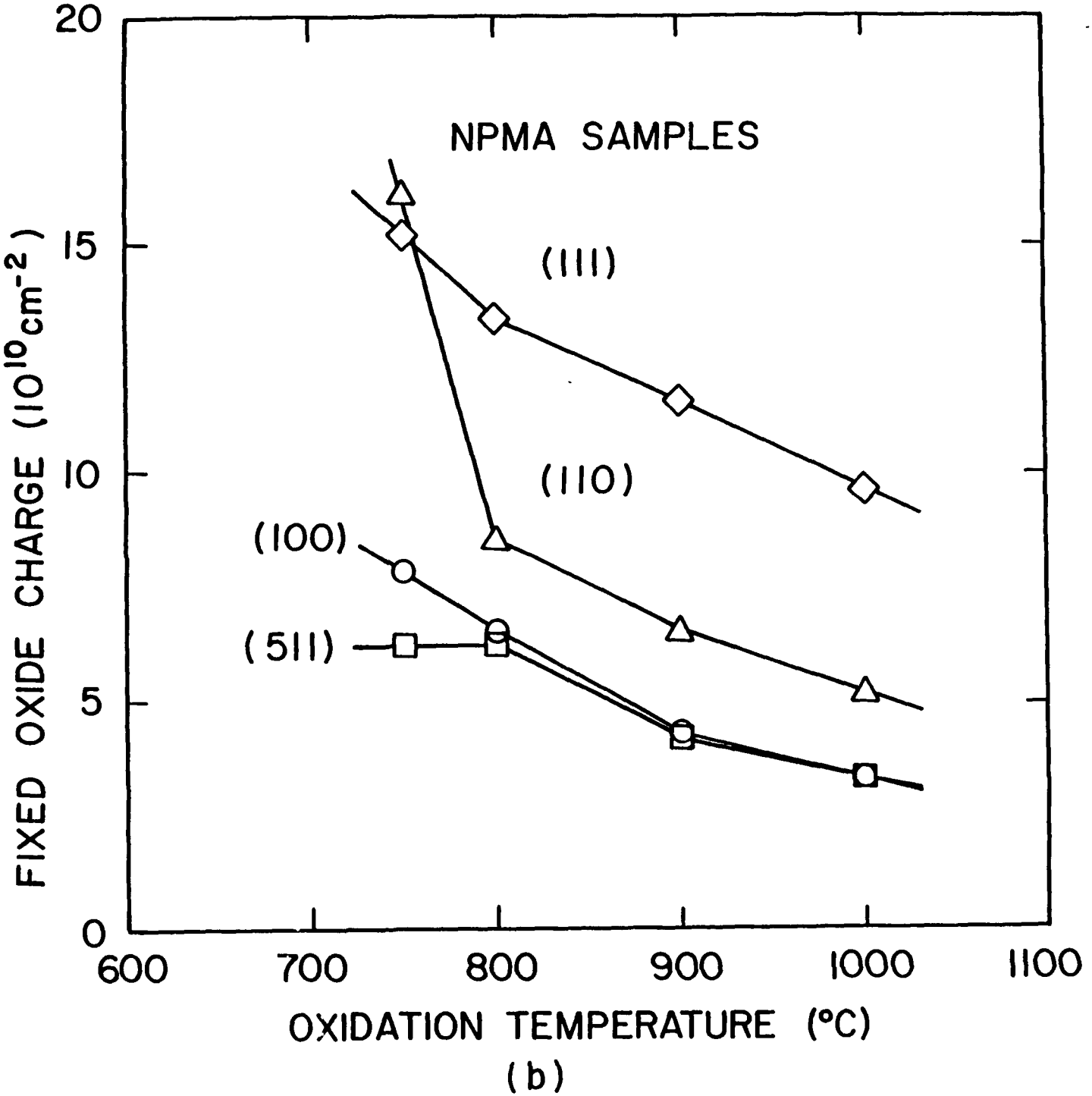



| F(T) | |
|---|---|
| INTRINSIC STRESS | $\sigma_i$ |
| DENSITY | $\rho$ |
| REFRACTIVE INDEX | n |
| FIXED OXIDE CHARGE | $Q_f$ |
| INTERFACE TRAP CHARGE | $Q_{it}$ |

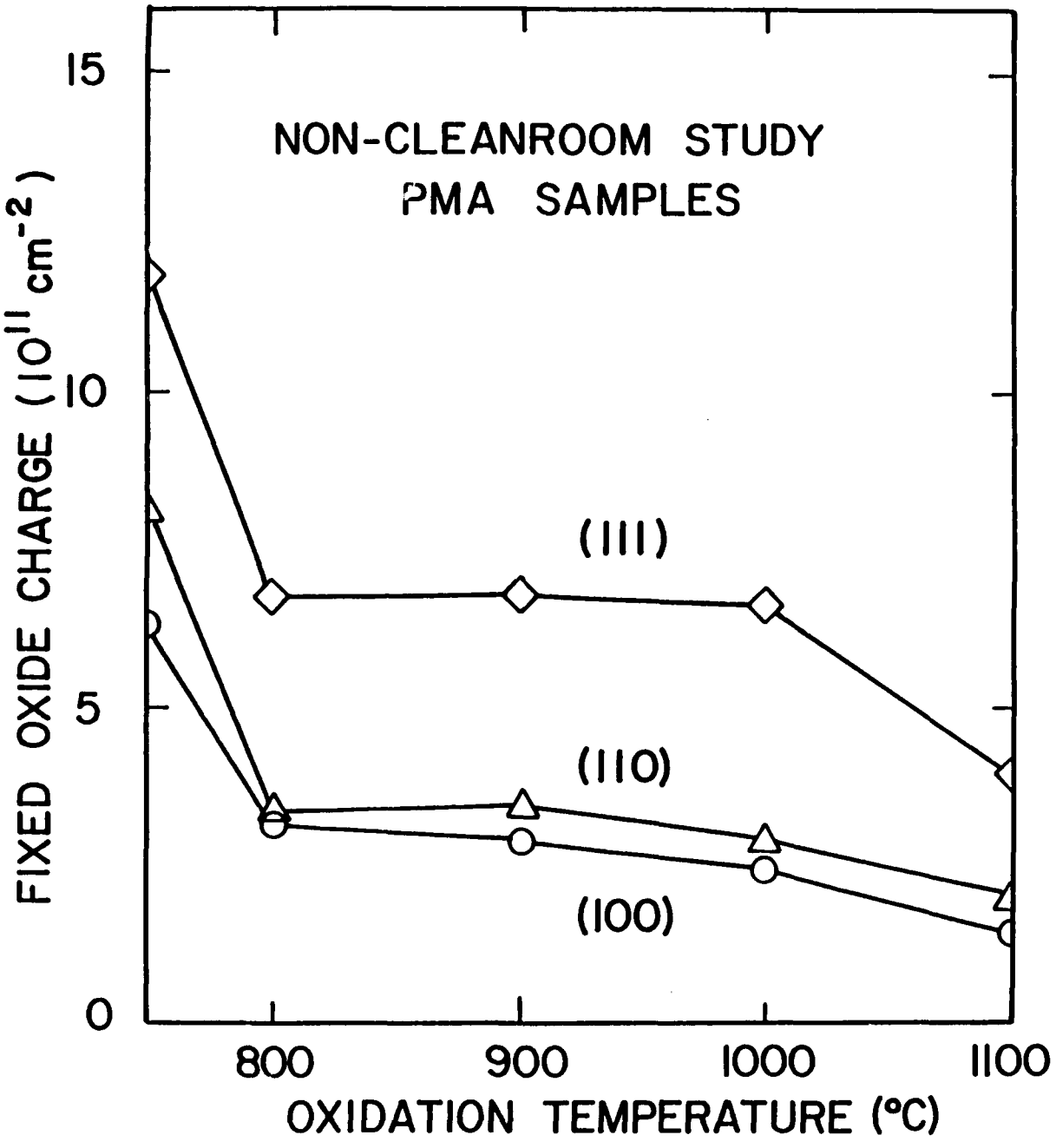

NPMA
PMA
INTERFACE TRAP DENSITY (cm⁻²eV⁻¹)
10¹²
10¹¹
E_V
E_C
0
0.2
0.4
0.6
0.8
1.0
BANDGAP ENERGY (eV)

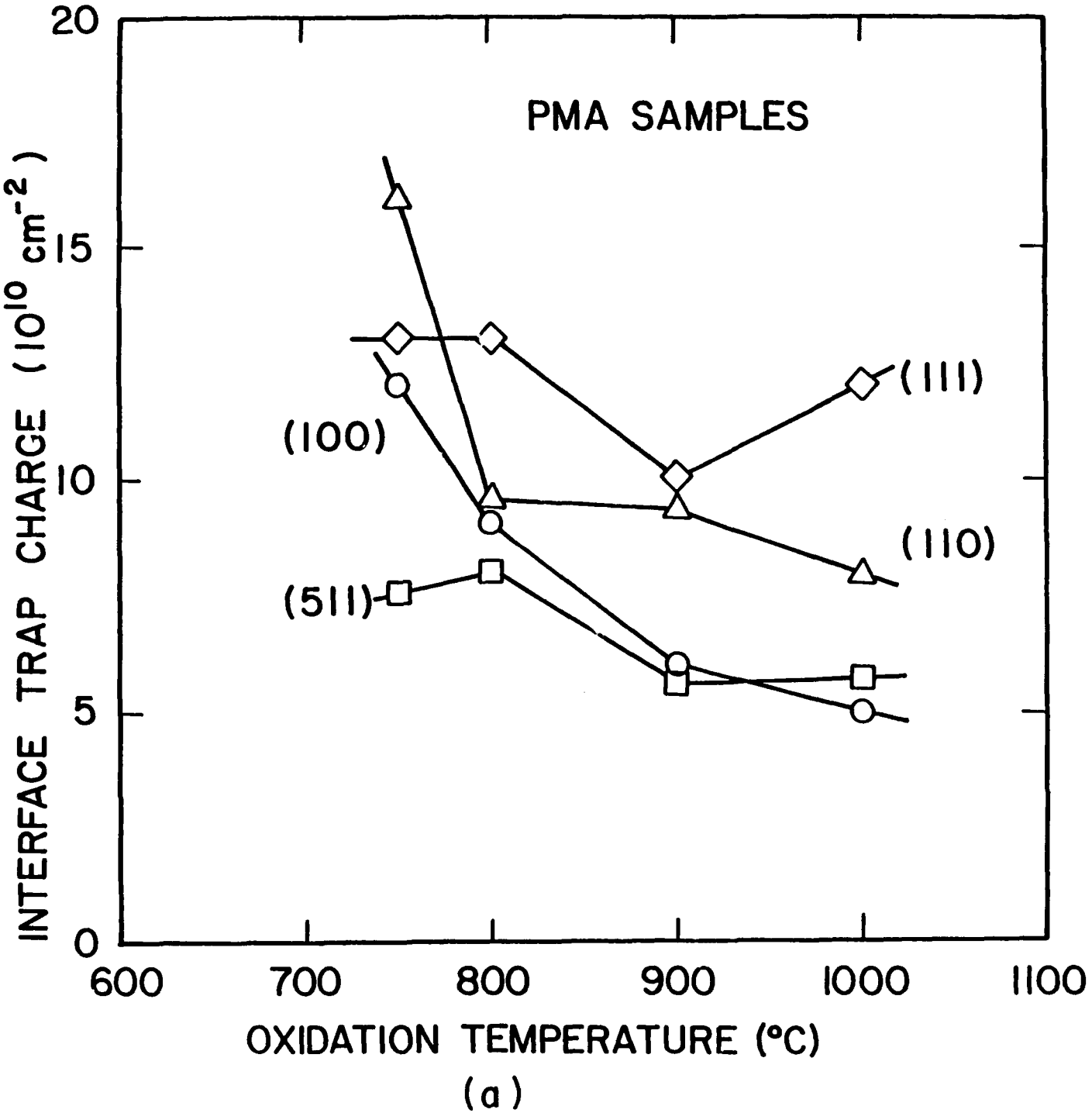

12
10
8
6
4
2
0
FIXED OXIDE CHARGE ( $10^{11}$ $cm^{-2}$ )
PMA SAMPLES
(110)
(111)
(511)
(100)
600
700
800
900
1000
1100
OXIDATION TEMPERATURE (°C)

(a)

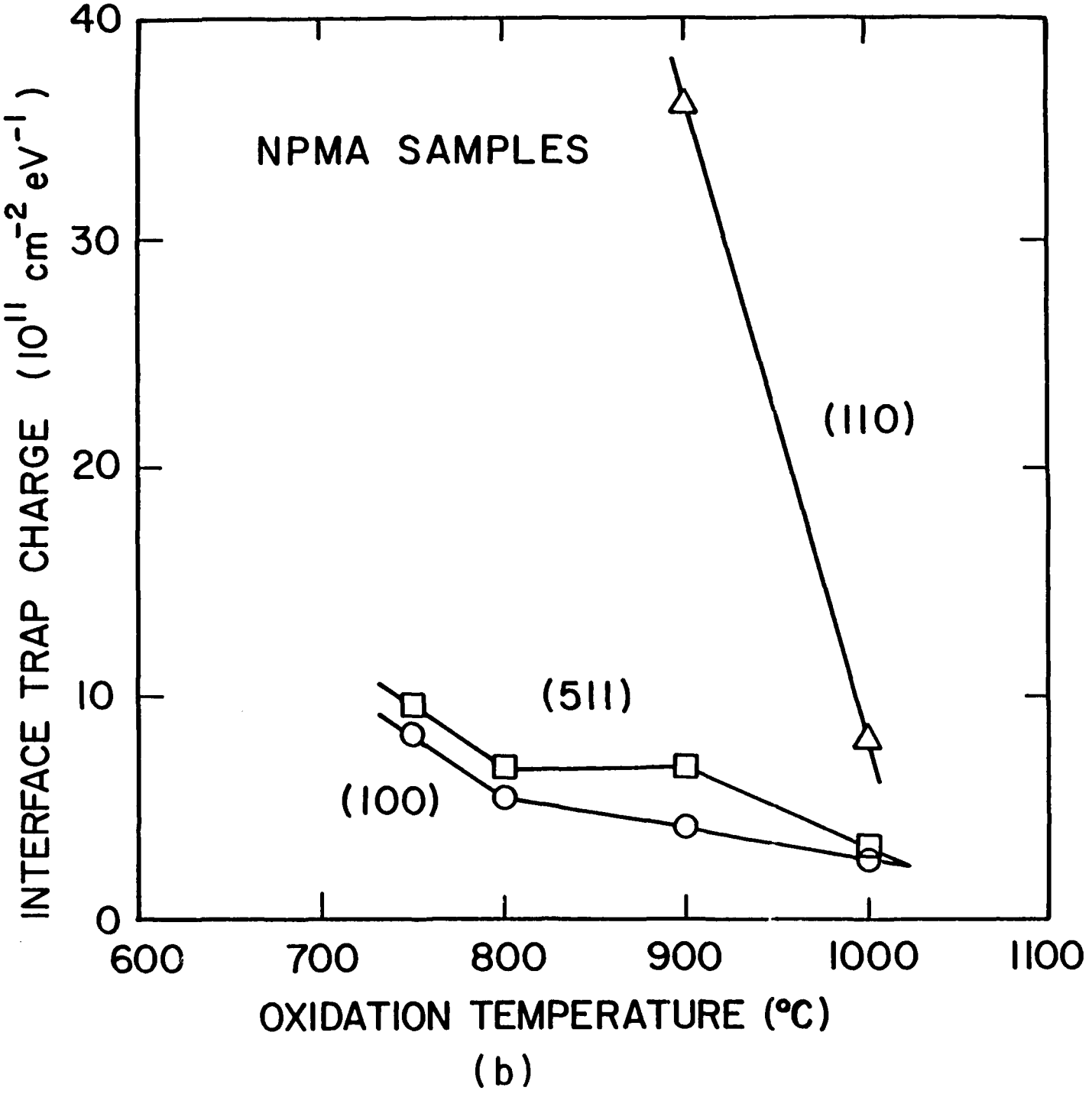

NPMA SAMPLES
(111)
(110)
(100)
(511)
FIXED OXIDE CHARGE ($10^{10}cm^{-2}$)
OXIDATION TEMPERATURE (°C)
0
5
10
15
20
600
700
800
900
1000
1100

(b)

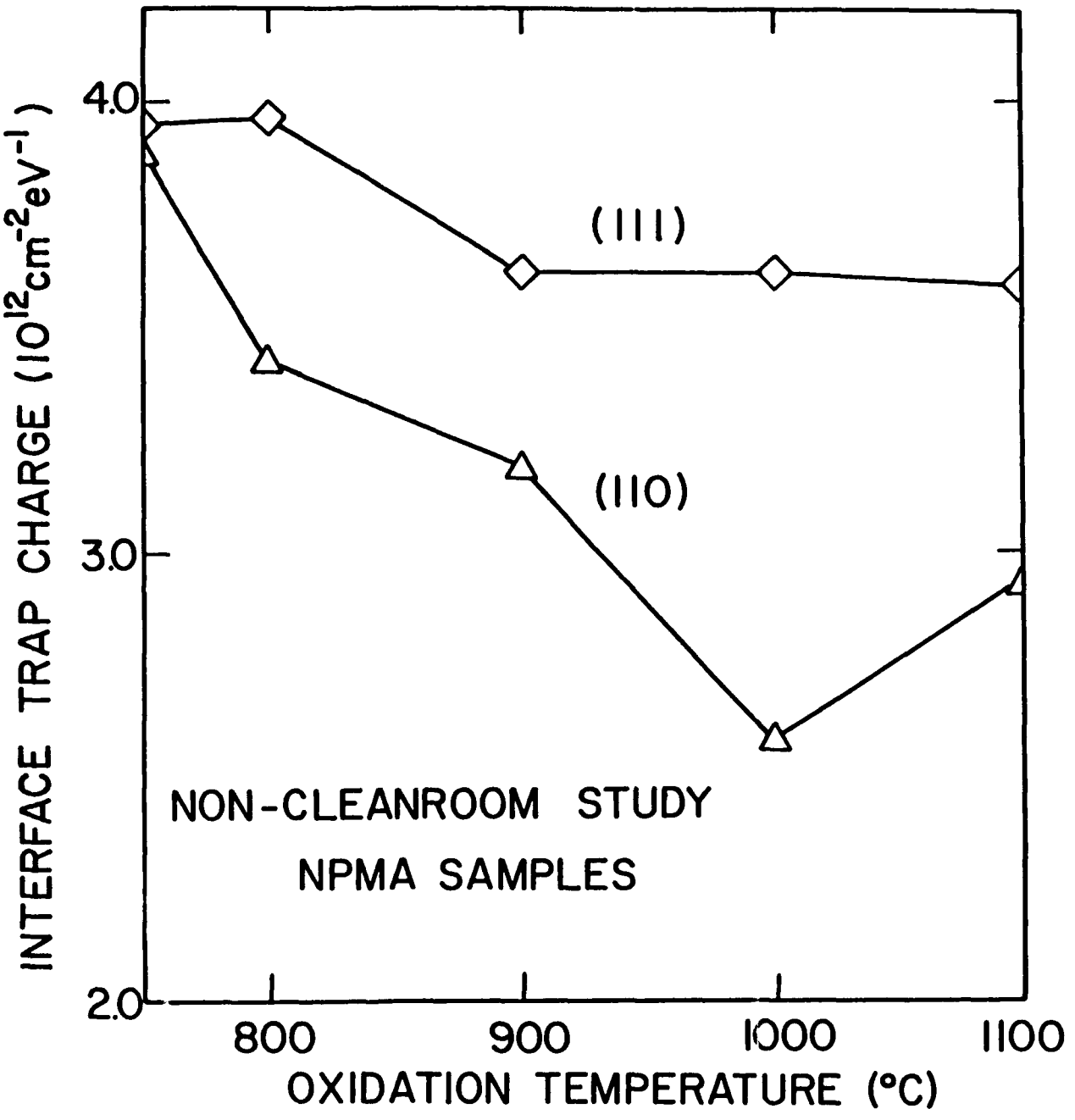

NON-CLEANROOM STUDY
PMA SAMPLES
FIXED OXIDE CHARGE ($10^{11}$ cm$^{-2}$)
15
10
5
0
(111)
(110)
(100)
800
900
1000
1100
OXIDATION TEMPERATURE (°C)

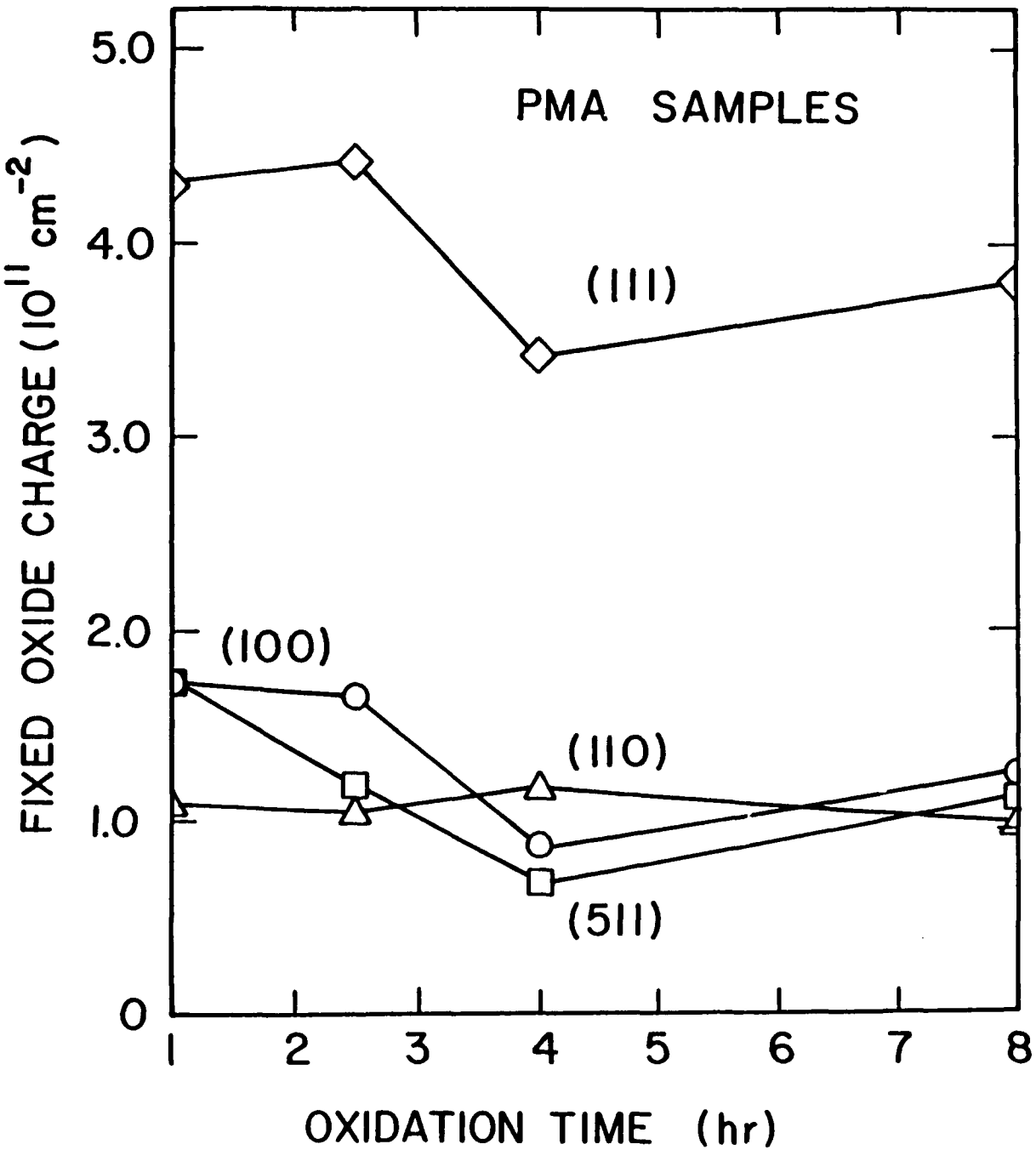

PMA SAMPLES
INTERFACE TRAP CHARGE ($10^{10}$ cm$^{-2}$)
OXIDATION TEMPERATURE (°C)
(111)
(110)
(100)
(511)
0
5
10
15
20
600
700
800
900
1000
1100

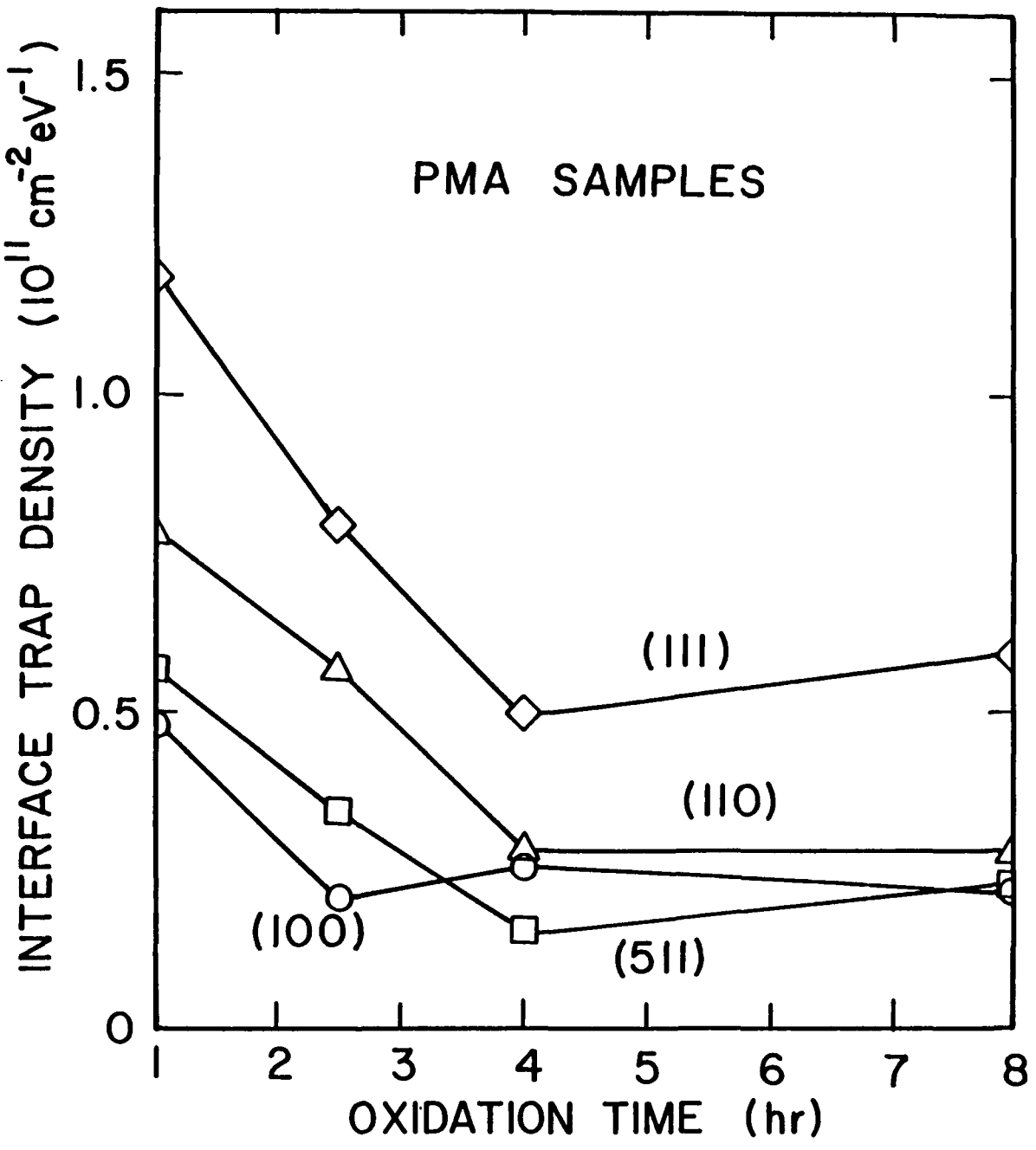
(a)

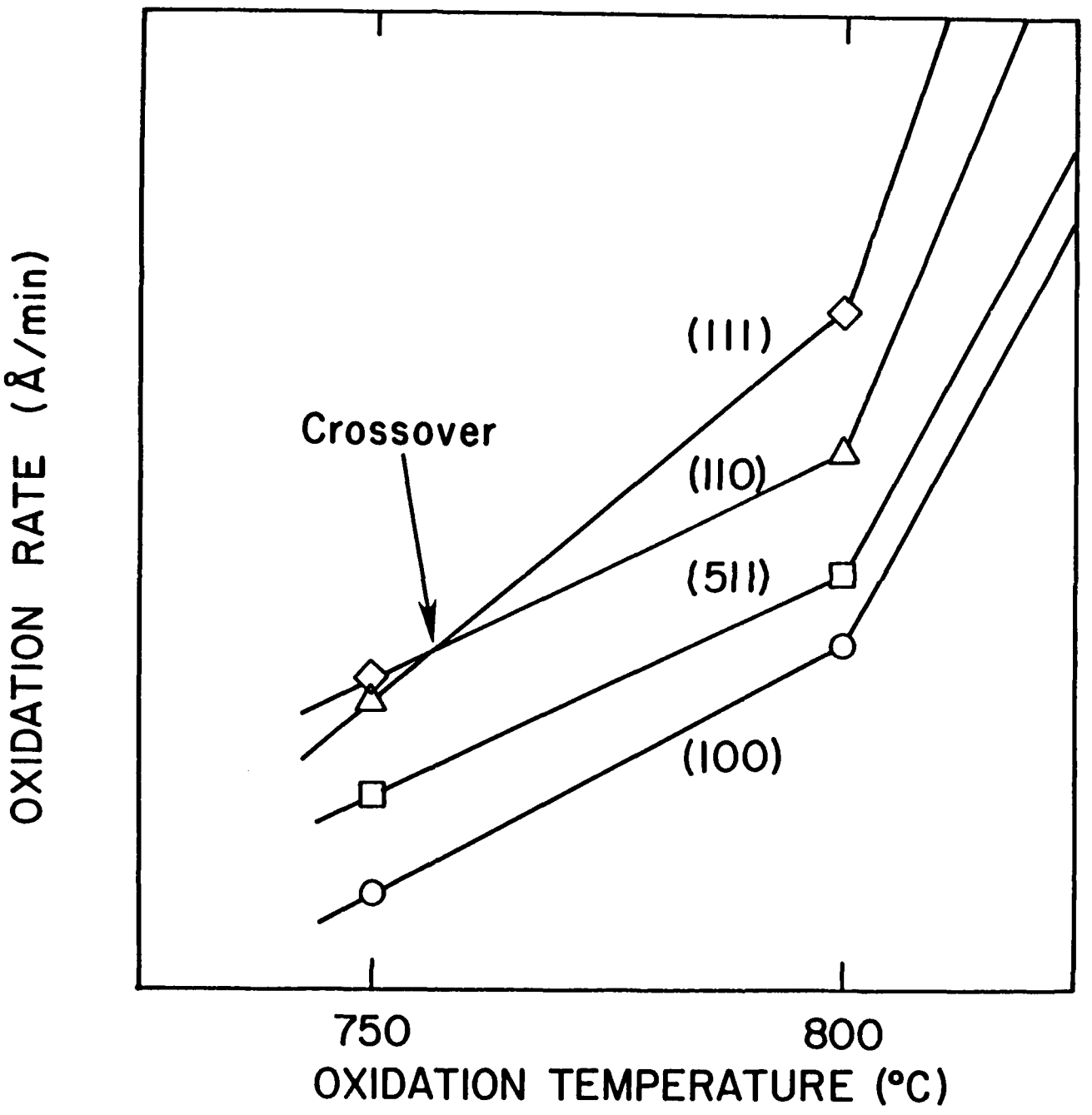

NPMA SAMPLES
(110)
(511)
(100)
INTERFACE TRAP CHARGE ($10^{11}$ $cm^{-2}$ $eV^{-1}$)
OXIDATION TEMPERATURE (°C)
0
10
20
30
40
600
700
800
900
1000
1100

(b)


INTERFACE TRAP CHARGE ($10^{12}cm^{-2}eV^{-1}$)
4.0
3.0
2.0
(111)
(110)
NON-CLEANROOM STUDY
NPMA SAMPLES
800
900
1000
1100
OXIDATION TEMPERATURE (°C)


PMA SAMPLES
(111)
(100)
(110)
(511)
FIXED OXIDE CHARGE ($10^{11}$ $cm^{-2}$)
OXIDATION TIME (hr)
5.0
4.0
3.0
2.0
1.0
0
1
2
3
4
5
6
7
8


PMA SAMPLES
INTERFACE TRAP DENSITY ($10^{11}$ cm$^{-2}$eV$^{-1}$)
1.5
1.0
0.5
0
1
2
3
4
5
6
7
8
OXIDATION TIME (hr)
(111)
(110)
(100)
(511)


OXIDATION RATE (Å/min)
(111)
Crossover
(110)
(511)
(100)
750
800
OXIDATION TEMPERATURE (°C)

## *LIST OF TABLES*

Table I. Oxidation temperatures and corresponding times used for each oxidation.

| Oxidation Temperature (°C) | Oxidation Time (hr) |
|---|---|
| Non-Cleanroom Conditions: (100), (110), and (111). | |
| 750 | 24.0 |
| 800 | 18.0 |
| 900 | 4.0 |
| 1000 | 1.0 |
| 1100 | 0.5 |
| Cleanroom Conditions: (100), (110), (111) and (511). | |
| 750 | 23.0 |
| 800 | 18.0 |
| 900 | 4.5 |
| 1000 | 8.0 |
| 1000 | 4.0 |
| 1000 | 2.5 |
| 1000 | 1.0 |

Table II. Comparison of fixed oxide charge and interface trap density for samples that were post-metallization annealed (PMA).

| | Oxidation Temperature (°C) | Fixed Oxide Charge Density $N_f$ ($10^{11}$ cm$^{-2}$) | | |
|---|---|---|---|---|
| | | (100) | (110) | (111) |
| Cleanroom Conditions: | 750 | 0.74 | 10.80 | 5.89 |
| | 800 | 1.60 | 1.92 | 4.99 |
| | 900 | 1.27 | 1.71 | 4.86 |
| | 1000 | 1.73 | 1.08 | 4.33 |
| Non-cleanroom Conditions: | 750 | 6.30 | 8.20 | 11.80 |
| | 800 | 3.12 | 3.35 | 6.73 |
| | 900 | 2.87 | 3.45 | 6.78 |
| | 1000 | 2.43 | 2.90 | 6.60 |
| | 1100 | 1.42 | 2.02 | 3.92 |
| Deal *et al.*[a)] | 920 | 1.70 | 2.10 | 4.70 |
| | 1200 | 0.20 | 0.60 | 1.70 |
| Razouk and Deal[b)] | 1000 | 0.80 | - | 3.30 |

a) Ref. 3.

b) Ref. 4.

| Oxidation Temperature (°C) | Interface Trap Charge Density $D_{it}$ at Midgap for (111) Si ($10^{11}$ cm$^{-2}$eV$^{-1}$) | |
|---|---|---|
| | Cleanroom Conditions: | Non-cleanroom Conditions: |
| 750 | 1.30 | 3.20 |
| 800 | 1.30 | 2.80 |
| 900 | 1.00 | 1.60 |
| 1000 | 1.20 | 4.90 |

Table III. Fixed oxide charge for post-metallization annealed (PMA) and non-post-metallization annealed (NPMA) samples.

| Oxidation Temperature (°C) | Cleanroom Fixed Oxide Charge Density $N_f$ ($10^{11}$ $cm^{-2}$) (Maximum Spread in Data Indicated as ±) | | | |
|---|---|---|---|---|
| | (100) | (511) | (110) | (111) |
| Post-metallization Annealed Samples (PMA) | | | | |
| 750 | 0.7±0.4 | 1.6±0.4 | 10.8±1.2 | 5.9±0.4 |
| 800 | 1.6±0.5 | 0.2±0.2 | 1.9±0.3 | 5.0±0.6 |
| 900 | 1.3±0.2 | 0.6±0.2 | 1.7±0.3 | 4.9±0.1 |
| 1000 | 1.7±0.1 | 1.8±0.1 | 1.8±0.1 | 4.3±0.2 |
| Non-Post-metallization Annealed Samples (NPMA) | | | | |
| 750 | 7.8±1.6 | 6.2±0.4 | 16.0±1.3 | 15.2±0.6 |
| 800 | 6.5±0.9 | 6.2±0.3 | 8.5±0.8 | 13.3±0.4 |
| 900 | 4.3±0.1 | 4.2±0.1 | 6.5±0.1 | 11.5±0.3 |
| 1000 | 3.3±0.3 | 3.3±0.3 | 5.1±0.5 | 9.6±0.6 |

Table IV. Interfac trap density for cleanroom post-metallization annealed (PMA) and non-post-metallization annealed (NPMA) samples.

| Oxidation Temperature (°C) | Cleanroom Interface Trap Density $D_{it}$ ($10^{11}$ $cm^{-2}eV^{-1}$) (Maximum Spread in Data Indicated as ±) | | | |
|---|---|---|---|---|
| | (100) | (511) | (110) | (111) |
| Post-metallization Annealed Samples (PMA) | | | | |
| 750 | 12.0±0.1 | 7.5±0.4 | 16.0±1.0 | 13.0±0.6 |
| 800 | 9.0±0.6 | 8.0±1.2 | 9.5±0.4 | 13.0±0.1 |
| 900 | 6.0±0.3 | 5.6±0.2 | 9.3±0.4 | 10.0±0.3 |
| 1000 | 5.0±0.1 | 5.7±0.1 | 7.9±1.0 | 12.0±0.6 |
| Non-Post-metallization Annealed Samples (NPMA) | | | | |
| 750 | 8.2±0.2 | 9.5±2.0 | 35.0±0.5[a)] | 22.0±—[a)] |
| 800 | 5.4±0.2 | 6.7±0.2 | 22.0±0.1[a)] | 16.0±—[a)] |
| 900 | 4.1±0.2 | 6.8±1.4 | 36.0±14[a)] | 14.0±—[a)] |
| 1000 | 2.6±0.1 | 3.2±0.2 | 8.0±1.2 | 11.0±—[a)] |

[a)] Values reported at 0.3 eV above the valence band where a minimum occurs.

Table V. The oxidation-temperature dependence of the slope of interface trap density ($D_{it}/T$) for non-post-metallization annealed (111) and (100) samples, in the 900–12–°C range from Ref. 4 and the 750–1000°C in this work.

| | $\Delta D_{it}/\Delta T$ ($10^{11}$ $cm^{-2}eV^{-1}K^{-1}$) | |
|---|---|---|
| | (111) | (100) |
| Razouk and Deal as oxidized.[a)] | −0.00433 | −0.030 |
| This Work, as-oxidized, cleanroom conditions. | −0.00488 | −0.023 |
| This Work, as-oxidized, non-cleanroom conditions. | −0.00314 | — |

a) Ref. 5.

Table VI. Fixed oxide charge $Q_f$ on samples oxidized at 1000°C with and without post-metallization annealing.

| Oxidation Time (hr) | Cleanroom Fixed Oxide Charge Density $N_f$ ($10^{11}$ cm$^{-2}$) | | | |
|---|---|---|---|---|
| | (100) | (511) | (110) | (111) |
| Post-metallization Annealed Samples (PMA) | | | | |
| 1.0 | 1.7 | 1.8 | 1.1 | 4.3 |
| 2.5 | 1.7 | 1.2 | 1.0 | 4.4 |
| 4.0 | 0.9 | 0.7 | 1.2 | 3.4 |
| 8.0 | 1.3 | 1.1 | 1.0 | 3.8 |
| Non-Post-metallization Annealed Samples (NPMA) | | | | |
| 1.0 | 3.3 | 3.3 | 5.1 | 9.6 |
| 2.5 | 2.8 | 2.5 | 4.3 | 8.9 |
| 4.0 | 2.8 | 2.8 | 3.4 | 8.0 |
| 8.0 | 3.0 | 3.0 | 3.9 | 8.4 |

Table VII. Interface trap charge $D_{it}$ on samples oxidized at 1000°C with and without post-metallization annealing.

| Oxidation Time (hr) | Interface Trap Charge Density $D_{it}$ at Midgap ($10^{10}$ $cm^{-2}eV^{-1}$) | | | |
|---|---|---|---|---|
| | (100) | (511) | (110) | (111) |
| Post-metallization Annealed Samples (PMA) | | | | |
| 1.0 | 4.9 | 5.7 | 7.9 | 12.0 |
| 2.5 | 2.1 | 3.4 | 5.7 | 7.9 |
| 4.0 | 2.6 | 1.5 | 2.8 | 5.0 |
| 8.0 | 2.2 | 2.3 | 2.8 | 6.0 |
| Non-Post-metallization Annealed Samples (NPMA) | | | | |
| 1.0 | 26 | 32 | 80 | 11 [a)] |
| 2.5 | 17 | 22 | 89 | 73 [a)] |
| 4.0 | 15 | 22 | 73 | 56 [a)] |
| 8.0 | 17 | 39 | 80 | 89 [a)] |

[a)] Measured at 0.3 eV above the valence band edge and not at midgap.

Table VIII. Ratios of the measured interface trap density $D_{it}$ and the silicon surface atom density $C_{Si}$ for the various orrientations oxidized at 750°C and post-metallization annealed.

| | (110)/(100) | (111)/(100) | (511)/(100) | (111)/(110) |
|---|---|---|---|---|
| ratios of $D_{it}$ | 1.30 | 1.10 | 0.63 | 0.81 |
| ratios of $C_{Si}$ | 1.40 | 1.15 | 0.63 | 0.86 |